INFORMATION DISCLOSURE CITATION

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ATTY. DOCKET NO. 540-127

SERIAL NO. 09/152,266 (To Be ~~Assigned~~)

APPLICANT CAMPBELL et al

FILING DATE 14 September 1998

GROUP

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TP		5,265,203	11/23/1993	PEASLEE et al			
TP		4.964,040	10/16/1990	WILCOX			
TP		4,905,175	2/27/1990	CORBETT et al			
TP		4,468,727	8/28/1984	CARRISON et al			

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
TP		0 362 903 A	4/11/1990	EUROPE			X	
TP		WO 91 16681 A	10/31/1991	WIPO			X	
TP		0 364 000 A	4/18/1990	EUROPE			X	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, etc.)

(7/15/05) TP		IBM TECHNICAL DISCLOSURE BULLETIN, vol. 28, no. 5, October 1985, NEW YORK US, pages 1981-1985, XP002034326 "Procedure for Hierarchical Chip Physical Design" see the whole document.
(7/15/05) TP		IEICE TRANSACTIONS ON ELECTRONICS, vol. E76-C, no. 11, November 1993, pages 1641-1648, XP000424603 NOBUTAR SHIBATA ET AL.: "HIGH-PERFORMANCE MEMORY MACROCELLS WITH ROW AND COLUMN SLICEABLE ARCHITECTURE" see abstract see page 1652, left-hand column, line 23; figures 1,2

*Examiner Thomas Phan | Date Considered 5/2/03

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

Form PTO-FB-A820 (Also PTO-1449